

## **EXHIBIT A**

## INVENTION DESCRIPTION

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Date: 2-12-2003

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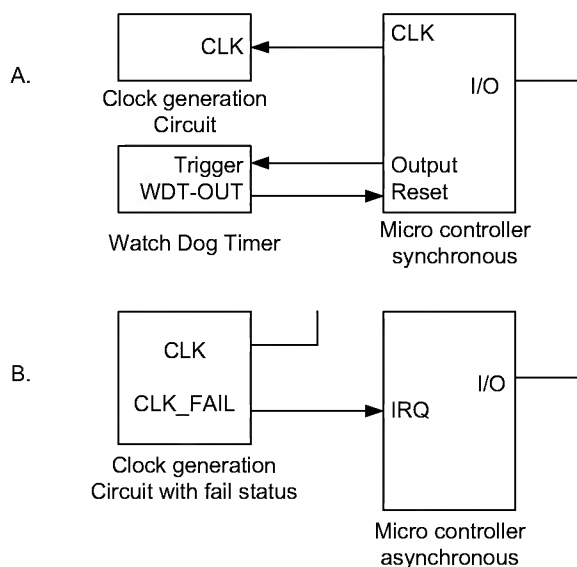
BX3.035, Tel: 024-3536392

## TITLE:

Failsafe principle: a failing clock source in an asynchronous circuit triggers a microcontroller to execute a "failsafe" software routine

## INVENTION DESCRIPTION

Normally when in a synchronously system a clock source stops functioning a microcontroller also stops with executing instructions because the clock edges are needed for instruction execution.



Pat-block1.vsd

Figure A. shows the synchronous failsafe principle. In normal operation mode the Watch Dog Timer (WDT) will be triggered regular, in case this triggering stops the WDT output will become active (after a defined period) and will reset the microcontroller

So this extra hardware is needed to 'execute' a failsafe event, for example a reset to turn off outputs and to reset the microcontroller.

By making use of asynchronous technology, whereby the clock generation circuit is not necessary for the execution of the microcontrollers instructions, extra hardware can be avoided to enter this failsafe event and this saves costs, refer to figure B.

In this case however a special clock source is necessary with a status output, which shows the status if the oscillator is running. By connecting this output to for example to an interrupt request input of the microcontroller, the microcontroller can detect the error condition.

This event will start a special software routine, which handles code related to a failing clock source without the need of the clock source.

So the advantage of this solution is: a dedicated software routine can be started to execute dedicated code and also having the possibility to modify this code.

**EMBODIMENT**

The principle of the described invention description is used in the UJA1023. This is a LIN I/O slave IC and makes use of asynchronous technology generated by TANGRAM. Inside this UJA1023 a microcontroller (type MRKII) and this special clock source with fail signal is used.

**FIELD OF APPLICATION**

Can be used generally with asynchronous microcontrollers.

**REMARK**

Please note samples of this UJA1023 will be shipped to customers in week 0403. A NDA is needed then.